1. An n-channel silicon JFET, comprising

a silicon substrate, having a top surface and a bottom surface;

a mono-crystalline silicon buried-layer near the top surface, doped with antimony to a concentration of about 1E19 atoms/cm^3;

the buried layer having a top surface;

a first mono-crystalline silicon region disposed on the top of the buried layer having a top surface and a bottom surface, doped with boron ions to a resistivity of about 7 ohms-cm, the distance between the top and the bottom surfaces being about 3.5 micrometers;

a first and second gate regions in the first silicon region each having a top surface, a bottom surface and a side surface, implanted with boron ions of about 6E12 ions/cm2 and at about 50 keV, communicable to a gate terminal near the top surface of the substrate;

the bottom surfaces of the first and second gate regions being substantially coplanar with the top surface of the buried layer and substantially parallel to and about 3.5 micrometers from the top surface of the first and second gate regions;

the first gate region having the shape of a bill-box having substantially flat and round top and bottom surfaces,

the second gate region having the shape of a concentric ring around the first gate region, having substantially flat and circular top and bottom surfaces substantially coplanar to the top and bottom surfaces of the first gate region,

a channel region disposed between the first and the second gate regions having the shape of a concentric ring, substantially flat top and bottom surfaces about 3.5 micrometers apart, and side surfaces substantially perpendicular to the top and bottom surfaces, implanted with phosphorous ions of about 1E13 ions/cm2 at about 900 keV and with boron ions of about 6E12 ions/cm2 at about 50 keV;

a drain region, disposed adjacent to the second gate region, having the shape of a concentric ring, substantially flat top and bottom surface about 3.5 micrometers apart, and side surfaces substantially perpendicular to the top and bottom surfaces, implanted with phosphorous ions of about 1E13 ions/cm2 at about 900 keV;

regions of silicon dioxide material having the shape of concentric rings electrically passivating boundary lines between the top surfaces of the gate regions, channel region, and drain region;

a source region atop a portion of the channel region;

metal elements contacting the top surfaces of the gate, source, and drain regions through a layer of silicide material, electrically communicable to external gate, source, drain terminals;

the n-channel JFET being operable passing an electric current in the channel region substantially in a direction perpendicular to the top surface of the substrate upon a biasing voltage applied between the source and the drain terminals; and

the magnitude of the channel current being controllable with a biasing voltage at the gate terminal.

2. An integrated-circuit device, comprising

a substrate, having a top surface and a bottom surface;

a first region near the top surface;

a first and second gate regions in the first region, each having a top surface, a bottom surface and a side surface;

the side surfaces of the first and second gate regions being substantially parallel to each other and substantially perpendicular to the top surface of the substrate;

the top surface of the first gate region being electrically communicable to a gate terminal;

a channel region in the first region, between the first and the second gate regions having side surfaces adjacent to the side surfaces of the gate regions, a top surface, and a bottom surface; and

the top surface of the channel region electrically communicable to a source terminal, the bottom surface of the channel region electrically communicable to a drain terminal.

3. The integrated-circuit device in claim 2, in which the channel region passes an electric current in a direction substantially perpendicular to the top surface of the substrate upon a biasing voltage being applied between the source terminal and the drain terminal, and the magnitude of the current in the channel region is controllable with a biasing voltage at the gate terminal.

4. The integrated-circuit device in claim 2, in which the substrate is p-type silicon.

5. The integrated-circuit device in claim 2, further comprising an n-type buried layer (NBL).

6. The integrated-circuit device in claim 5, in which the NBL is doped with antimony.

7. The integrated-circuit device in claim 2, in which the first region is formed by an epitaxial growth technique.

8. The integrated-circuit device in claim 7, in which the epi layer is n-type.

9. The integrated-circuit device in claim 2, in which the substrate is a bonded wafer.

10. The integrated-circuit device in claim 2, in which the first gate region has a pill-box shape with a substantially flat top surface and bottom surface and a side surface substantially perpendicular to the top and bottom surfaces.

11. The integrated-circuit device in claim 10, in which the channel region has a ring shape enclosing the first gate region, a bottom surface substantially coplanar to the bottom surface of the first gate region and a top surface substantially coplanar to the top surface of the first gate region.

12. The integrated-circuit device in claim 11, in which the second gate region has a ring shape enclosing the channel region, a bottom surface substantially coplanar to the bottom surface of the first gate region and a top surface substantially coplanar to the top surface of the first gate region.

13. The integrated-circuit device in claim 12, in which the drain plug region has a ring shape enclosing the second gate region, a bottom surface substantially coplanar to the bottom surface of the first gate region and a top surface substantially coplanar to the top surface of the first gate region.

14. The integrated-circuit device in claim 13, in which gate-, source-, and drain-contact areas are formed on the top surfaces of the gate-, channel-, and drain-region respectively.

15. The integrated-circuit device in claim 14, in which metal leads are formed connecting a gate contact area to a gate terminal, a source contact to a source terminal, and a drain contact area to a drain terminal.

16. A method for making an n-channel silicon JFET, comprising

providing a silicon substrate, having a top surface and a bottom surface;

forming a mono-crystalline silicon buried-layer near the top surface, doped with antimony to a concentration of about 1E19 atoms/cm^3;

growing a epitaxial, silicon first-layer on the top of the buried layer, doped with boron ions to a resistivity of about 7 ohms-cm, the thickness of the first layer being about 3.5 micrometers, the first layer having a top surface and a bottom surface;

forming a first and second gate regions in the first region by selectively implanting the regions with boron ions of about 6E12 ions/cm2 and at about 50 keV, each gate region having a top surface, a bottom surface and a side surface, the bottom surfaces of the first and second gate regions being substantially coplanar with a top surface of the buried layer and substantially parallel to and about 3.5 micrometers from the top surface of the first and second gate regions;

the first gate region having the shape of a bill-box having substantially flat and round top and bottom surfaces,

the second gate region having the shape of a concentric ring enclosing the first gate region, having substantially flat and circular top and bottom surfaces substantially coplanar to the top and bottom surfaces of the first gate region,

forming a channel region between the first and the second gate regions by implanting phosphorous ions of about 1E13 ions/cm2 at about 900 keV and with boron ions of about 6E12 ions/cm2 at about 50 keV, the channel region having the shape of a concentric ring enclosing the first gate region, a substantially flat top-surface and bottom surface about 3.5 micrometers apart, and side surfaces substantially perpendicular to the top and bottom surfaces,;

forming a drain region adjacent to the second gate region by implanting phosphorous ions of about 1E13 ions/cm2 at about 900 keV, the drain region

having the shape of a concentric ring enclosing the second gate region, substantially flat top surface and bottom surface about 3.5 micrometers apart, and side surfaces substantially perpendicular to the top and bottom surfaces;

forming regions of silicon dioxide material atop the gate regions, channel region, and drain region, electrically passivating the boundaries between the gate regions and the channel regions; and between the gate regions and the drain region;

forming a source-, gate-, and drain-contact areas atop a portion of the channel-, gate-, and drain-region respectively; and

forming metal-lead elements connecting the a source-contact area to a source terminal; a gate-contact area to a gate terminal; and a drain-contact area to a drain terminal.